PRE-DRIVE CIRCUIT FOR BRUSHLESS DC SINGLE-PHASE MOTOR

This is a Continuation of Application No. 10/265,717 filed October 8, 2002. The entire disclosure of the prior application is hereby incorporated by reference herein in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a brushless DC single-phase motor ideally used as a fan motor for exhausting the heat generated in a cabinet of electronic equipment to the outside. More particularly, the present invention relates to a pre-drive circuit for applying control signals to a switching device of a drive circuit of the brushless DC single-phase motor.

2. Description of the Related Art

[0002] In electronic equipment, including office automation equipment, typically represented by a personal computer and copying machine, that accommodates a number of electronic parts in a relatively small cabinet, the heat generated from the electronic parts is confined in the cabinet, leading to a danger of the electronic parts being thermally damaged.

[0003] To solve such a problem, a vent hole is provided in a wall surface or a ceiling surface of the cabinet of such electronic equipment, and a fan motor is installed at the vent hole so as to exhaust the heat in the cabinet to the outside.

[0004] For such a fan motor, a brushless DC single-phase motor is used frequently. A conventional pre-drive circuit for the brushless DC single-phase motor will be described with reference to Fig. 3.

[0005] Referring to Fig. 3, the pre-drive circuit is defined by the section of the brushless DC single-phase motor excluding a coil (motor coil) L1 and a drive circuit 31 therefor. Vcc denotes a DC power source for operating the circuit.

[0006] As shown in the drawing, the drive circuit 31 is constituted by four switching devices, namely, n-channel MOS power field-effect transistors (FETs) PF1 through PF4, a diode D31, and a capacitor C31.

[0007] The coil L1 is provided on a stator (not shown) of the motor, and energized at a predetermined ON/OFF timing by the four power FETs PF1 through PF4 of the drive circuit 31, which drives the coil L1, so as to produce a dynamic magnetic field or a rotating magnetic field.

[0008] A rotor (not shown) of the motor is provided with a permanent magnet, and rotated as the permanent magnet rotates, following the magnetic field.

[0009] The pre-drive circuit is constructed of dedicated integrated circuits IC1 and IC2, resistors R31 through R35, capacitors C32 through C35, and diodes D32 through D35. The power FETs, PF1 through PF4, have parasitic diodes, as shown in the drawing.

[0010] In the following descriptions, the dedicated integrated circuits IC1 and IC2 will be referred to simply as the dedicated IC1 and IC2, and the power FETs, PF1, PF2, PF3, and PF4, will be referred to simply as PF1, PF2, PF3, and PF4.

[0011] The dedicated IC1 receives a rotational position signal x of a motor, i.e., a rotor or permanent magnet, detected by a Hall element or the like (not shown), a high-level signal y for shutdown, and a duty ratio setting signal z for controlling the rotational speed of the motor. The dedicated IC1 is subjected to a step-up voltage VB1, which will be discussed hereinafter, to turn ON or OFF the PF1 and PF3 at timings set on the basis of the signals x, y, and z.

[0012] The signals x, y, and z are also supplied to the dedicated IC2. Upon receipt of a step-up voltage VB2, which will be discussed hereinafter, the dedicated IC2 turns ON or OFF the PF2 and PF4 at timings set on the basis of the signals x, y, and z.

[0013] Of the PF1 through PF4 connected as illustrated, the PF3 and PF4 turn ON if the potentials of their gates, i.e., control input terminals, are slightly higher than a ground potential, because their sources are grounded. The PF1 and PF2 are adjacent to a power source Vcc with the coil L1 installed therebetween. Hence, in a normal mode wherein the drive voltage of the coil L1 is substantially equal to a power supply voltage (Vcc), a voltage exceeding the power supply voltage must be applied to their gates. In other words, a voltage obtained by adding the gate-source voltage required for turning the PF1 and PF2 ON to the power supply voltage must be applied to the gates.

[0014] Capturing such voltage higher than the power supply voltage from outside inevitably adds to the complication and size of a power supply circuit, as well as higher cost. For this reason, it is usually desired to obtain such a voltage within the pre-drive circuit itself.

[0015] As a solution to the above problem, a step-up circuit, such as a charge pump circuit, is added. Each of the circuit constituted by the diode D32, the capacitor C34, and the resistor R31, and the circuit constituted by a diode D33, the capacitor C35, and the resistor R31 makes up the charge pump circuit.

[0016] In this case, a step-up voltage VB1 from a connection point of the diode D32 and the capacitor C34 is applied to the dedicated IC1 as a step-up voltage VB for turning the PF1 ON. Similarly, a step-up voltage VB2 from a connection point of the diode D33 and the capacitor C35 is applied to the dedicated IC2 as a step-up voltage VB for turning the PF2 ON.

[0017] Thus, the dedicated IC1 supplies a high-voltage pulse signal HO based on the voltage VB to the gate of the PF1 at a predetermined ON/OFF timing. Similarly, the

dedicated IC2 supplies the high-voltage pulse signal HO based on the voltage VB to the gate of the PF2 at a predetermined ON/OFF timing. On the other hand, low-voltage pulse signals LO based on the power supply voltage (Vcc) are supplied from the dedicated IC1 and IC2 to the gates of the PF3 and PF4 at predetermined ON/OFF timings.

[0018] The ON/OFF timings are set in the dedicated IC1 and IC2 on the basis of the signals x, y, and z. The signals from the dedicated IC1 and IC2 cause the PF1 through PF4 to turn ON or OFF at predetermined timings and duty ratios so as to control the energization of the coil L1.

[0019] Thus, the motor, i.e., the rotor, rotates in a predetermined direction at a speed based on the signals x, y, and z. If the motor is equipped with a fan and installed at the vent hole in the cabinet of electronic equipment, then the motor operates as a fan motor to exhaust the heat in the cabinet to the outside.

[0020] The conventional circuit, however, uses the dedicated IC1 and IC2, which are costly.

[0021] Furthermore, the use of the dedicated IC1 and IC2 restricts the gate voltages of the PF1 and PF2 adjacent to the power source to the values within a fixed range.

[0022] To be more specific, as mentioned above, the gate voltages of the PF1 and PF2 must be higher than the power supply voltage. The voltages are obtained by a charge pump circuit or the like, and applied to the gates of the PF1 and PF2 by the dedicated IC1 and IC2 on the basis of the voltages applied as the step-up voltages VB1 and VB2 to the VB terminals, namely, the step-up voltage input terminals, of the dedicated IC1 and IC2. However, the ICs, namely, the dedicated IC1 and IC2, are housed in a single package, and the circuit configuration therein is fixed. This means that the range of the step-up voltages VB1 and VB2 applied to the VB terminals of the PF1 and PF2, i.e., the range wherein the

gate voltages of the PF1 and PF2 can be changed, depends on the specifications of the ICs, and therefore cannot be arbitrarily changed.

[0023] Hence, the degree of freedom in the circuit design involving the ICs is unavoidably limited, making it impossible to permit flexible circuit design that involves, for example, a change of a motor to be driven, a change of the rated drive voltage of the motor coil L1, or a change of the power FETs (the PF1 through PF4) themselves, that would cause a change in the gates voltages of the PF1 and PF2. Especially if a change is made to increase the gate voltages (step-up voltages) of the PF1 and PF2, failure to pay attention to the rating of the step-up voltage input terminals when applying the increased voltages would present a problem of damaging the dedicated IC1 and IC2.

SUMMARY OF THE INVENTION

[0024] The present invention has been made with a view toward solving the problem described above, and it is an object of the invention to provide a pre-drive circuit for a brushless DC single-phase motor that can be constructed at low cost, and permits the control input voltage of a switching device adjacent to a power source to be easily changed or adjusted in a wider range without causing damage to a circuit element even when a change is made to increase the control input voltage.

[0025] To this end, according to the present invention, there is provided a pre-drive circuit for a brushless DC single-phase motor having a drive circuit in which a pair of series connected units, each series connected unit being constituted by two switching devices, is connected between a power source and the ground, a motor coil connected between the junctions of the two switching devices of the pair of series connected units can be controllably energized/de-energized from any direction at any timing by controlling the turning ON/OFF of the switching devices, a control voltage exceeding a power supply voltage is required to turn ON the two switching devices adjacent to a power source, and a

duty ratio of a turning ON/OFF control voltage applied to the switching devices is changed to control the rotational speed of the motor, the pre-drive circuit including: a step-up circuit for boosting a power supply voltage to a predetermined voltage; a logic circuit for generating and outputting pulse signals for controlling the switching devices on the basis of a motor rotational position signal and a duty ratio setting signal for controlling a motor rotational speed; two switching device drive circuits adjacent to the power source that are respectively connected to pulse signal output terminals for controlling the two switching devices adjacent to the power source of the logic circuit, respectively receive step-up voltages from the step-up circuit as operating power sources, respectively amplify the pulse signals for controlling the two switching devices adjacent to the power source to a predetermined voltage level exceeding the power supply voltage, and respectively supply the amplified pulse signals to control input terminals of the two switching devices adjacent to the power source; and two switching device drive circuits adjacent to the ground that are respectively connected to the pulse signal output terminals for controlling the two switching devices adjacent to the ground of the logic circuit, respectively receive voltages that are the power supply voltage or less as operating power sources, respectively amplify the pulse signals for controlling the two switching devices adjacent to the ground as necessary, and supply the amplified pulse signals to the control input terminals of the two switching devices adjacent to the ground.

[0026] Preferably, the step-up circuit includes a potentiometer that allows the step-up voltage to be set by setting a resistance value. A desired step-up voltage is obtained by setting the resistance value of the potentiometer on the basis of a control voltage value required for turning ON the two switching devices adjacent to the power source.

[0027] Preferably, the switching device drive circuit adjacent to the power source has a resistor and an NPN transistor and a PNP transistor that are connected in series in a

forward direction through the intermediary of the resistor. The bases of the two transistors are commonly connected to the output terminals of the pulse signals for controlling the switching devices, which are adjacent to the power source, of the logic circuit, while the end of the resistor adjacent to the ground is connected to the control input terminal of the switching device adjacent to the power source.

[0028] Preferably, the switching device drive circuit adjacent to the ground has a resistor and an NPN transistor and a PNP transistor that are connected in series in a forward direction through the intermediary of the resistor. The bases of the two transistors are commonly connected to the output terminals of the pulse signals for controlling the switching devices, which are adjacent to the ground, of the logic circuit, while the end of the resistor adjacent to the ground is connected to the control input terminal of the switching device adjacent to the ground.

[0029] Preferably, the pre-drive circuit for a brushless DC single-phase motor further includes an overvoltage protection circuit for restraining an overvoltage between the control input terminal of the switching device adjacent to the power source and the switching end, which is adjacent to a motor coil, of a pair of switching ends of the switching device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] Fig. 1 is a circuit diagram showing an embodiment in accordance with the present invention.

[0031] Fig. 2 is a circuit diagram showing another embodiment in accordance with the present invention.

[0032] Fig. 3 is a circuit diagram showing a conventional circuit.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0033] An embodiment of the present invention will now be described with reference to the accompanying drawings.

[0034] Fig. 1 is a circuit diagram showing a drive circuit for a brushless DC single-phase motor in accordance with an embodiment of the present invention.

[0035] A pre-drive circuit is defined by the portion of the circuit shown in Fig. 1 that excludes a coil, namely, a motor coil, L1 of the brushless DC single-phase motor, and a drive circuit 31. Vcc denotes a DC power source for operating the circuit. In this example, the operating power source of the coil L1 comes from the power source Vcc; alternatively however, a separate power source may be provided for operating the coil L1.

[0036] The drive circuit 31 is constituted by four switching devices, namely, n-channel MOS power field-effect transistors (FETs) PF1 through PF4, a diode D31, and a capacitor C31, as shown in the diagram.

[0037] The four power FETs PF1 through PF4 are divided into two power FET series connected units (a series connected unit constructed of the PF1 and PF3, and another series connected unit constructed of the PF2 and PF4). The connected units are respectively connected between the power source Vcc and the ground, the polarities thereof being as illustrated. The diode D31 is connected between the power source Vcc and the two series connected units (the series connected unit of the PF1 and PF3, and the series connected unit of PF2 and PF4) in the forward direction with respect to the power source Vcc. The capacitor C31 is connected between the cathode of the diode D31 and the ground. The coil L1, which is to be driven, is connected between the connection point of the PF1 and the PF3 and the connection point of the PF2 and PF4.

[0038] The coil L1 is provided on a stator of the motor (not shown), and energized by the PF1 through PF4 at predetermined ON/OFF timings to produce a dynamic magnetic field or a rotating magnetic field.

[0039] A rotor (not shown) of the motor is equipped with a permanent magnet, and rotated as the permanent magnet rotates, following the magnetic field.

[0040] The pre-drive circuit in accordance with the present invention is constructed of a logic circuit 17 (17a through 17d) including, for example, four AND circuits 11 through 14 and two inverter circuits 15 and 16, resistors R11 through R30, R41 and R42, capacitors C11 through C15, diodes D11 through D13, zener diodes ZD1 through ZD4, NPN transistors T1 through T4, and PNP transistors T5 through T8. The power FETs, PF1 through PF4, have parasitic diodes, as shown in the drawing.

[0041] Based on signals x, y, and z similar to those shown in Fig. 3, the logic circuit 17 outputs signals (voltage waveforms) similar to the signals output from the dedicated IC1 and IC2 shown in Fig. 3 so as to turn ON/OFF the PF1 through PF4 at the timings set on the basis of the signals x, y, and z. In this embodiment, the logic circuit 17 is constituted by a general-purpose IC that includes four or more AND circuits and two or more inverter circuits.

[0042] As previously mentioned, of the PF1 through PF4 connected as illustrated, the PF3 and PF4 have their sources grounded, so that they turn ON if the gates serving as control input terminals have a slightly higher potential than the ground potential. The PF1 and PF2 are located adjacently to the power source Vcc with the coil L1 provided therebetween. Hence, in a normal mode wherein the drive voltage of the coil L1 is substantially equal to a power supply voltage (Vcc), a voltage exceeding the power supply voltage must be applied to their gates. In other words, a voltage obtained by adding the gate-source voltage required for turning the PF1 and PF2 ON to the power supply voltage must be applied to the gates. Capturing such voltage higher than the power supply voltage from outside inevitably adds to the complication and size of a power supply circuit, as well as higher cost. For this reason, it is usually desired to obtain such a voltage within the pre-drive circuit itself.

[0043] As a solution to the above problem, a step-up circuit, such as a charge pump circuit, is added. A charge pump circuit 18 formed of a diode D11, a capacitor C15, and resistors R41 and R42 (potentiometer) constitutes the charge pump circuit.

[0044] More specifically, in the charge pump circuit 18 according to this embodiment, a resistor R41, a forward diode D11, and a capacitor C15 are connected in this order from the power source Vcc between the power source Vcc and the source of the PF1, and a resistor R42 is connected between the connection point of the resistor R41 and the diode D11 and the ground.

[0045] According to the charge pump circuit 18, if the resistance values of the resistors R41 and R42 making up the potentiometer are denoted as R41 and R42, and the voltage value of the power source Vcc is denoted as Vcc, then a step-up voltage VB obtained by $\{R42/(R41+R42)\} \cdot Vcc$ is output from the connection point of the diode D11 and the capacitor C15.

[0046] The transistors T1 and T5 and a resistor R19, and transistors T2 and T6 and a resistor R20 constitute PF drive circuits 19 and 22, respectively, adjacent to the power source. The PF drive circuits 19 and 22 amplify pulse signals for controlling the two PFs adjacent to the power source to a predetermined voltage level exceeding a power supply voltage Vcc, that is, at least a voltage level at which the PF1 and PF2 adjacent to the power source can be turned ON.

[0047] To be more specific, in the PF drive circuit 19 adjacent to the power source, the transistors T1 and T5 connected in series in the forward direction through the intermediary of the resistor R19 are interposed between a DC power source terminal VB, to which the step-up voltage VB is applied, and the ground. In this case, the bases of the two transistors T1 and T5 are commonly connected to a terminal PO1 for outputting pulse signals for controlling the PF1 adjacent to the power source of the logic circuit 17a. The end of the resistor R19 that is adjacent to the ground, i.e., the point between the resistor

R19 and the emitter of the transistor T5, is connected to the gate of the PF1 adjacent to the power source (the control input terminal).

[0048] In this embodiment, the end of the resistor R19 that is adjacent to the ground is connected to the gate of the PF1 adjacent to the power source through the intermediary of an overvoltage protection circuit 20 for the gate-source of the PF1 adjacent to the power source, which is constituted by resistors R23 and R24 and a zener diode ZD1. The commonly connected bases of the transistors T1 and T5 are connected to the terminal PO1 for outputting pulse signals through the intermediary of a noise protection filtering circuit 21 formed of resistors R12 and R11 and a capacitor C11.

[0049] In a PF drive circuit 22 adjacent to the power source, the transistors T2 and T6 connected in series in the forward direction through the intermediary of a resistor R20 are interposed between the DC power source terminal VB, to which the step-up voltage VB is applied, and the ground. In this case, the bases of the two transistors T2 and T6 are commonly connected to a terminal PO2 for outputting pulse signals for controlling the PF2 adjacent to the power source of the logic circuit 17b. The end of the resistor R20 that is adjacent to the ground, i.e., the point between the resistor R20 and the emitter of the transistor T6, is connected to the gate of the PF2 adjacent to the power source.

[0050] In this embodiment, the end of the resistor R20 that is adjacent to the ground is connected to the gate of the PF2 adjacent to the power source through the intermediary of an overvoltage protection circuit 23 for the gate-source of the PF2 adjacent to the power source, which is constituted by resistors R25 and R26 and a zener diode ZD2. The commonly connected bases of the transistors T2 and T6 are connected to the terminal PO2 for outputting pulse signals through the intermediary of a noise protection filtering circuit 24 formed of resistors R14 and R13 and a capacitor C12.

[0051] The transistors T3 and T7, a resistor R21, and a diode D12, and transistors T4 and T8, a resistor R22, and a diode 13 constitute PF drive circuits 25 and 28,

respectively, adjacent to the ground. The PF drive circuits 25 and 28 amplify pulse signals for controlling the two PFs adjacent to the ground to an appropriate value of the power supply voltage Vcc or less, basically to the gate-source (ground) voltage value at which the PF3 and PF4 adjacent to the ground can be turned ON.

[0052] To be more specific, in the PF drive circuit 25 adjacent to the ground, the transistors T3 and T7 connected in series in the forward direction through the intermediary of a resistor R21 are interposed between the DC power source Vcc and the ground. In this case, the bases of the two transistors T3 and T7 are commonly connected to a terminal PO3 for outputting pulse signals for controlling the PF1 adjacent to the ground of the logic circuit 17c. The end of the resistor R21 that is adjacent to the ground, i.e., the point between the resistor R21 and the emitter of the transistor T7, is connected to the gate of the PF3 adjacent to the ground.

[0053] In this embodiment, the end of the resistor R21 that is adjacent to the ground is connected to the gate of the PF3 adjacent to the ground through the intermediary of an overvoltage protection circuit 26 for the gate-source of the PF3 adjacent to the ground, which is constituted by resistors R27 and R28 and a zener diode ZD3. The commonly connected bases of the transistors T3 and T7 are connected to the terminal PO3 for outputting pulse signals through the intermediary of a noise protection filtering circuit 27 formed of resistors R16 and R15 and a capacitor C13. The DC power source Vcc is connected to the collector of a transistor T3 through the intermediary of a forward diode D12.

[0054] In a PF drive circuit 28 adjacent to the ground, transistors T4 and T8 connected in series in the forward direction through the intermediary of a resistor R22 are interposed between the DC power source Vcc and the ground. In this case, the bases of the two transistors T4 and T8 are commonly connected to a terminal PO4 for outputting pulse signals for controlling the PF4 adjacent to the ground of the logic circuit 17d. The

end of the resistor R22 that is adjacent to the ground, i.e., the point between the resistor R22 and the emitter of the transistor T8, is connected to the gate of the PF4 adjacent to the ground.

[0055] In this embodiment, the end of the resistor R22 that is adjacent to the ground is connected to the gate of the PF4 adjacent to the ground through the intermediary of an overvoltage protection circuit 29 for the gate-source of the PF4 adjacent to the ground, which is constituted by resistors R29 and R30 and a zener diode ZD4. The commonly connected bases of the transistors T4 and T8 are connected to the terminal PO4 for outputting pulse signals through the intermediary of a noise protection filtering circuit 30 formed of resistors R18 and R17 and a capacitor C14. The DC power source Vcc is connected to the collector of a transistor T4 through the intermediary of a forward diode D13.

[0056] The operation of the foregoing circuit in accordance with the present invention will now be described.

[0057] Based on signals x, y, and z similar to those shown in Fig. 3, the logic circuit 17 (17a through 17d) outputs signals (voltage waveforms) similar to the signals output from the dedicated IC1 and IC2 shown in Fig. 3 to the pulse signal output terminals PO1 through PO4.

[0058] To be more specific, signals similar to pulse signals HO of the dedicated IC1 are supplied to the pulse signal output terminal PO1, and signals similar to pulse signals LO are supplied to the pulse signal output terminal PO3. Furthermore, signals similar to the pulse signals HO of the dedicated IC2 are supplied to the pulse signal output terminal PO2, and signals similar to the pulse signals LO are supplied to the pulse signal output terminal PO4.

[0059] The pulse signals output to the pulse signal output terminals PO1 and PO2 are amplified to a voltage level (high voltage level), at which the PF1 and PF2 adjacent to

the power source can be turned ON, by the PF drive circuits 19 and 22 adjacent to the power source that receive the step-up voltage VB from the charge pump circuit 18 as their operating power sources. The amplified pulse signals are supplied to the gates of the PF1 and PF2 adjacent to the power source.

[0060] The pulse signals output to the pulse signal output terminals PO3 and PO4 are amplified to a voltage level (low voltage level), at which the PF3 and PF4 adjacent to the ground can be turned ON, by the PF drive circuits 25 and 28 adjacent to the ground that receive a voltage of the power supply voltage Vcc or less (the power supply voltage Vcc in this case) as their operating power sources. The amplified pulse signals are supplied to the gates of the PF3 and PF4 adjacent to the ground.

[0061] It is assumed that a normal rotation mode is set when the coil L1 is energized from the left end toward the right end in the drawing (a ventilation mode when the motor is applied to a fan motor) and that a 100% duty ratio is set in this direction. In other words, it is assumed that signals for running at a maximum speed are being output from the logic circuit 17 (17a through 17d) to the pulse signal output terminals PO1 through PO4. In this case, high-level pulse signals are being supplied to the pulse signal output terminals PO1 and PO4, while low-level pulse signals are being supplied to the pulse signal output terminals PO2 and PO3.

[0062] At this time, a high-level pulse signal to the pulse signal output terminal PO1 is supplied to the PF drive circuit 19 adjacent to the power source to turn ON the NPN transistor T1 thereof. The high-level pulse signal is amplified to a high-voltage level of the power supply voltage Vcc or more before it is supplied to the gate of the PF1 to turn the PF1 ON.

[0063] The high-level pulse signal to the pulse signal output terminal PO4 is supplied to the PF drive circuit 28 adjacent to the ground to turn ON the NPN transistor T4 thereof. The high-level pulse signal is amplified to a low-voltage level of the power

supply voltage Vcc or less that is sufficient to turn the PF4 ON (amplification factor 1 is included in this case). The amplified pulse signal is then supplied to the gate of the PF4 to turn the PF4 ON.

[0064] Meanwhile, low-level signals are being output to the pulse signal output terminals PO2 and PO3, placing the PF drive circuits 22 and 25 in an inactive mode wherein the transistors T2 and T3 are both OFF over the full period.

[0065] Thus, current I from the DC power source Vcc passes along a route of the diode D31, the PF1 (drain-source), the coil L1, the PF4 (drain-source), and the ground in this order, as indicated by a solid-line arrow I, for each high-level duration of the pulse signal to the pulse signal output terminals PO1 and PO4. The rise and fall of the turning ON of the PF1 and PF4 are always simultaneous as long as the duty ratio is set to 100%, and the motor (the rotor) runs at the maximum speed. This means that, when the motor is applied to a fan motor, maximum ventilation is performed to exhaust the heat in the cabinet of electronic equipment provided with the fan motor to the outside at a maximum capacity.

[0066] The rise and fall timings of the pulse signals supplied to the pulse signal output terminals PO1 and PO4 are based on the rotational position signal x of the motor (the rotor or the permanent magnet) that is detected by a Hall device or the like (not shown).

[0067] If the motor runs at a duty ratio below 100%, e.g., at 50% speed, then only the falling timing of the pulse signal supplied to the pulse signal output terminal PO4 will be advanced by a half, as compared with the timing when the duty ratio is 100%. In other words, the high-level duration of the pulse signal supplied to the pulse signal output terminal PO4 is reduced by half without causing a change in the high-level duration of the pulse signal supplied to the pulse signal output terminal PO1.

[0068] Thus, the duration in which the current from the DC power source Vcc passes along the route of the diode D31, the PF1 (drain-source), the coil L1, the PF4 (drain-source), and the ground in this order will be the half the duration at the above 100% duty ratio. The motor, therefore, runs at half the maximum speed.

[0069] During the ON period of the PF1, which is longer than the ON period of the PF4, that is, during the period in which only the PF1 is ON while the PF4 is OFF, current I' from the coil L1 is absorbed by a capacitor C3 through the parasitic diode of the PF2, as indicated by a dash-line arrow I'. The electric charges absorbed by the capacitor C3 will be released when the PF1 is turned ON next.

[0070] The diode D31 serves as a backflow blocker for blocking the current from the coil L1 from flowing toward the DC power source Vcc. The capacitor C3 functions also as a noise remover.

[0071] If the high-level pulse signals are supplied to the pulse signal output terminals PO2 and PO3, while the low-level signals are supplied to the pulse signal output terminals PO1 and PO4, then the PF1 and the PF4 turn OFF, while the PF2 and the PF3 turn ON. This causes the coil L1 to be energized from the right end toward the left end in the drawing, and the motor runs in the reverse direction. When the motor runs in the reverse direction, the PF2 and the PF3 operate in the same manner as the PF1 and the PF4 operate when the motor runs in the normal direction. The coil L1 is energized at a predetermined duty ratio based on the pulse signals x, y, and z supplied to the pulse signal output terminals PO2 and PO3 so as to rotate the motor.

[0072] Fig. 2 is a circuit diagram showing another embodiment of the present invention.

[0073] In Fig. 2, the same or equivalent components as or to the components shown in Fig. 1 will be assigned the same reference numerals. This embodiment is

obtained by removing the overvoltage protection circuits 26 and 29 and the noise protection filtering circuits 27 and 30 from the circuit shown in Fig. 1.

[0074] A lower voltage is applied to the gates of the PF3 and PF4 adjacent to the ground, and it is less likely for an overvoltage to be developed between the gates and sources. Hence, the overvoltage protection circuits 26 and 29 may be omitted. There are less noises at the pulse signal output terminals PO3 and PO4, so that the noise protection filtering circuits 27 and 30 may be also omitted.

[0075] In the above embodiments, the n-channel MOS power FETs have been used as the switching devices; however, the present invention is not limited thereto. Alternatively, for example, power transistors may be used, in which diodes are in antiparallel connection between the collectors and emitters thereof.

[0076] The charge pump circuits have been used as the step-up circuits for supplying voltages exceeding the power supply voltage to the switching device drive circuits adjacent to the power source. Alternatively, however, bootstrap circuits or the like may be used.

[0077] Thus, the present invention provides the following advantages. The circuit equivalent to the dedicated ICs in the conventional circuit has been configured using mere logic circuits, such as AND circuits, OR circuits, and inverter circuits (the AND circuits and the inverter circuits in the above embodiments). This permits the use of circuit elements, such as transistors and diodes, and inexpensive circuits, such as general-purpose ICs, making the circuits to be configured at lower cost.

[0078] Furthermore, the switching device drive circuit has been connected to the output terminal of such a logic circuit. More specifically, the switching device drive circuit has been configured separately and independently from the logic circuit, and connected to the logic circuit. If the logic circuit is constituted by a general IC, then the switching device drive circuit is externally attached to the logic circuit. This arrangement

has eliminated the restrictions that the dedicated IC of the conventional circuit has in the voltage range of the operating power source of the switching device drive circuit, especially the range of the step-up voltage from a step-up circuit applied as the operating power source for the switching device drive circuit adjacent to the power source. Hence, the freedom in circuit designing has been improved, providing flexibility in making various changes, including the change of the motor to be driven. This means that a change of the rated drive voltage of a motor coil or a switching device itself, which involves a change of the control input voltage of the switching device (especially an increase in the control input voltage) can be made without damaging any circuit element.

[0079] Moreover, the step-up circuit has been configured using the potentiometer that allows the step-up voltage to be set by setting the resistance value. With this arrangement, a desired step-up voltage based on a control voltage value required to turn ON the two switching devices adjacent to the power source can be easily obtained simply by selecting a resistance value.

[0080] Furthermore, the switching device drive circuit adjacent to the power source can be configured using a simple circuit that includes a resistor and an NPN transistor and a PNP transistor connected in series in the forward direction through the intermediary of the resistor.

[0081] Similarly, the switching device drive circuit adjacent to the ground can be configured using a simple circuit that includes a resistor and an NPN transistor and a PNP transistor connected in series in the forward direction through the intermediary of the resistor. The configuration of the switching device drive circuit adjacent to the ground is similar to the switching device drive circuit adjacent to the power source; therefore, both switching device drive circuits can be designed and fabricated at the same time, although they require slightly different parameters, such as resistance values. This permits a reduction in cost to be achieved.

[0082] In addition, the overvoltage protection circuit has been provided between the control input terminal of the switching device adjacent to the power source and the switching terminal, which is adjacent to the motor coil, of the pair of switching terminals of the switching device. This arrangement makes it possible to protect the switching device adjacent to the power source that is more prone to be subjected to an overvoltage than the switching device adjacent to the ground. Thus, the reliability of the pre-drive circuit can be improved.